

# TPA3123D2 Audio Power Amplifier EVM

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#### 1 Introduction

The TPA3123D2 evaluation module consists of a single 25-W, class-D, stereo audio power amplifier complete with a small number of external components mounted on a circuit board that are used to directly drive speakers with an external analog audio source as the input.

Table 1. TPA3123D2 EVM Specifications

		VALUE	UNIT
V <sub>CC</sub>	Supply voltage range	10 to 30	V
I <sub>CC</sub>	Supply current, maximum	2	Α
Po	Continuous output power, $P_O$ : 4 $\Omega$ , $V_{CC}$ = 27 V, THD+N = 10%	24	W
$Z_{L}$	Minimum load impedance	3.2	Ω

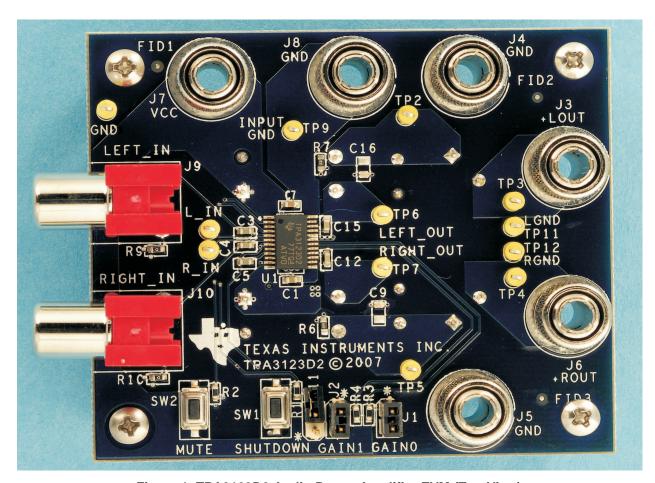


Figure 1. TPA3123D2 Audio Power Amplifier EVM (Top View)



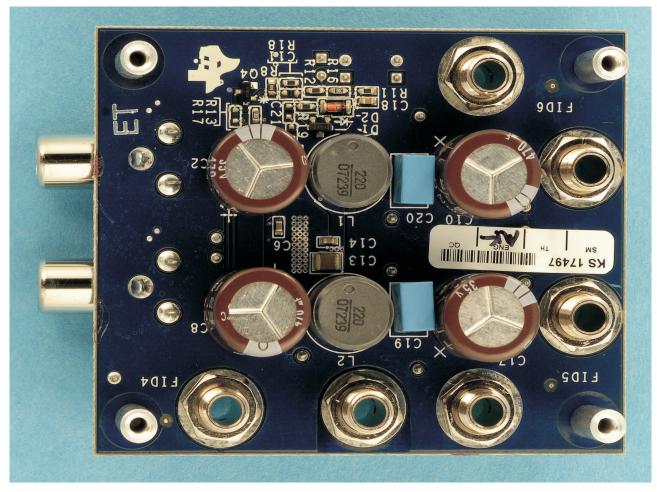


Figure 2. TPA3123D2 Audio Power Amplifier EVM (Bottom View)



#### 2 Operation

#### 2.1 Quick Start List for Stand-Alone Operation

Follow these steps to use the TPA3123D2EVM stand-alone or when connecting it into existing circuits or equipment. Connections to the EVM module can be made by inserting stripped wire, or using banana plugs for the power supply and output connections. The inputs accept standard RCA plugs.

### 2.1.1 Power Supply

- 1. Ensure that all external power sources are set to OFF.
- 2. Connect an external regulated power supply adjusted from 10 V to 30 V to the module VCC (J7) and GND (J8) banana jacks taking care to observe marked polarity.

#### 2.1.2 Evaluation Module Preparations

Inputs and Outputs:

- 1. Connect an audio source to the input jacks, **J9** and **J10**.
- 2. Connect a speaker across GND (J5) and +ROUT (J6). Connect another speaker across LOUT (J3) and GND (J4)
- 3. Install both gain jumpers GAIN0 (J1) and GAIN1 (J2). This sets the gain of the amplifier to the lowest level, 20 dB.

#### Control Inputs:

- 1.  $\overline{\text{SHUTDOWN}}$ : This terminal is active LOW. A LOW on the device terminal (<0.8 V) shuts down the amplifier; a HIGH (>2 V) on the device terminal places the amplifier in the active state. Holding down switch SW1 places the amplifier in the SHUTDOWN state. Releasing SW1 returns the amplifier to the active state. This terminal is  $V_{CC}$  compliant.
- 2. MUTE: This terminal is active HIGH. A HIGH (>2 V) on this terminal will immediately terminate audio playback through the speakers; a LOW (<0.8 V) enables the device. The outputs remain switching with fifty percent duty cycle. SW2 on the EVM controls the state of the MUTE terminal. Holding down switch SW2 places the amplifier in the MUTE state. Releasing SW2 returns the amplifier to the active state. This terminal is V<sub>CC</sub> compliant.
- 3. **GAIN0/GAIN1**: Together, these terminals determine the gain of the amplifier. See Table 2. Installing a jumper in J1 or J2 sets the respective terminal to GND. Removing the jumper sets the respective terminals to VCC. Removing jumpers *increases* the gain while installing jumpers *decreases* the gain. Logic levels are TTL compatible. These terminals are V<sub>CC</sub> compliant.
- 4. Power-off Depop Circuit: Additional circuitry to quiet power-off pop is provided on the EVM. This circuit consists of shunt regulator D1, bipolar transistor Q4, and the surrounding components. This circuit is activated by installing the jumper J11 which connects V<sub>CC</sub> to the network. The depop circuit has two different modes of operation. When R13 is installed, this circuit slowly pulls down the voltage on the Bypass pin when power is removed resulting in a controlled reduction of the Class D output duty cycle. If R17 is installed, the network reduces the pop by pulling down the shutdown pin at power-off. This approach can be used if the power supply operates in such a way that there is a significant time delay between removal of power and the point where V<sub>CC</sub> falls below the chip UVLO level, which is approximately 8 volts.

**Table 2. Gain Settings** 

GAIN0 (J1)	GAIN1 (J2)	Amplifier Gain (dB)
ON	ON	20
ON	OFF	26
OFF	ON	32
OFF	OFF	36



# 2.1.3 Power Up

1. Verify correct voltage and input polarity, and turn the external power supplies ON.

The EVM should begin operation.

- 1. Adjust the input signal.
- 2. Adjust the control inputs to the desired settings.
- 3. Adjust the amplifier gain by installing/removing the gain jumpers, J1 and J2.

#### 3 TPA3123D2 EVM Schematic

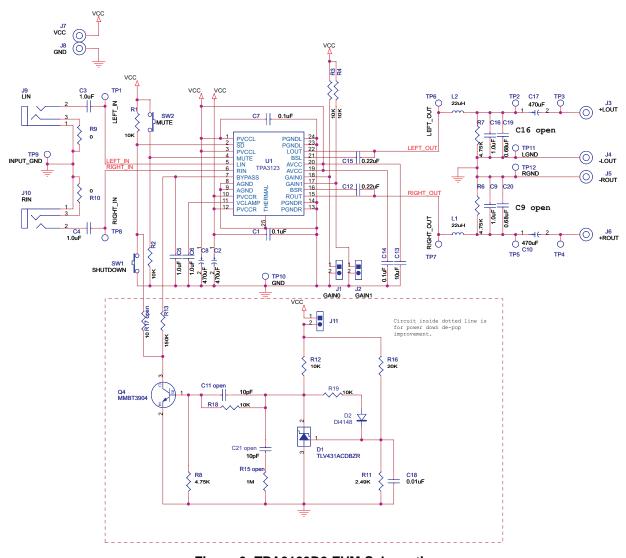


Figure 3. TPA3123D2 EVM Schematic



# 4 TPA3123D2 EVM PCB Layers

The following illustrations depict the TPA3123D2 EVM PCB layers.

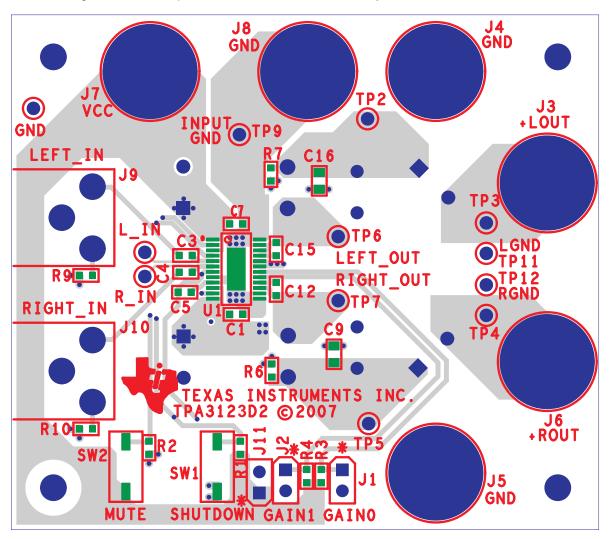


Figure 4. Top Side Layout



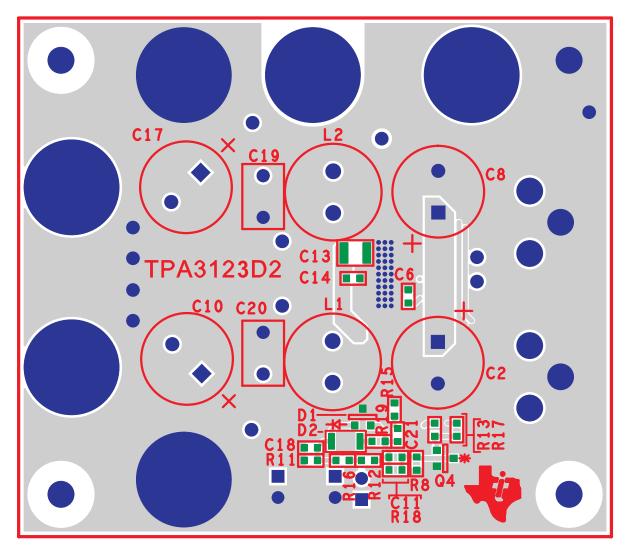


Figure 5. Bottom Side Layout



# 5 TPA3123D2 Evaluation Module Parts List

# Table 3. TPA3123D2 EVM Bill of Materials

Ref.	Description	Size	Qty	Status	Manufacturer	Part Number
C1, C7, C14	Capacitor, ceramic, 0.1 µF, ±10%, X7R, 50V	0603	3		TDK	C1608X7R1H104KT
C2, C8, C10, C17	Capacitor, Electrolytic, 470 μF, 35 V	Radial	4		Nichicon	UHE1V471MH06
C3-C6	Capacitor, ceramic, 1.0 µF, ±10%, X7R, 16V	0603	4		Taiyo Yuden	EMK107BJ105KA-TR
C9, C16	Capacitor, ceramic, 1.0 µF, ±10%, X7R, 50V	0805	2	open	TDK	C3216X7R1H105K
C12, C15	Capacitor, ceramic, 0.22 μF, ±10%, X7R, 16V	0603	2		TDK	C1608X7R1C224KT
C13	Capacitor, ceramic, 10 μF, +80%/–20%, Y5V, 50V	1210	1		Murata	GRM32DF51H106ZA01L
C19, C20	Capacitor, metal poly, 0.68 μF, 63V	Radial	2		EPCOS, Inc.	B32529C684J
L1-L2	Inductor, 22 µH, radial lead, ferrite material, shielded	Radial	2		Toko	A7503AY-220M
R1-R4	Resistor, chip, 10 kΩ, 1/16 W, 5%	0603	4		Panasonic	ERA-V15J103V
R6, R7	Resistor, chip, 4.7 kΩ, 1/10 W, 5%	0603	2		Panasonic	ERJ-3GEYJ472V
R9, R10	Resistor, chip, 0 Ω, 1/10 W, 5%	0603	2		Panasonic	ERJ-3GEY0R00V
J1-J2	Phono Jack, PC mount, switched		2		Switchcraft	PJRAN1X1U03
J3-J8	Banana Jack w/knurled Thumbnut (nickel plate)		6		Johnson	111-2223-001
J9-J10	Header, 2 position, Male	2mm	2		Norcomp	2163-36-01-P2
JP9-JP10 (shunts)	SHUNT, 2MM	2mm	2		Specialty	2JM-G
SW1, SW2	Switch, momentary, SMD, Low profile		2		Panasonic	EVQ-PPBA25
	Standoffs, 5/8" length, 4-40 thread		4		Keystone	1808
	Screws, 4-40, .375		4			
U1	TPA3123D2PWP	24 pin TSSOP	1		TI	TPA3123D2PWP
The following p	arts comprise the power-off depop circuit w	hich is enabled	by insta	lling J11.		
C11, C21	Capacitor, ceramic, 10 pF, ±10%, C0G, 100V	0603	2	open	Murata	GRM1885C2A100RA01D
C18	Capacitor, ceramic, 0.01 μF, ±10%, X7R, 50V	0603	1		TDK	C1608X7R1H103K
D1	Shunt Regulator, Adjustable	SOT-23-3	1		Texas Instruments	TLV431ACDBZR
D2	Rectifier, Silicon, 0.15 A, 75V	mini MELF	1		Micro Commercial	DL4148-TP
Q4	Transistor, NPN, AMP	SOT-23	1		Fairchild Semiconductor	MMBT3904
R8	Resistor, chip, 4.7 kΩ, 1/10 W, 5%	0603	1		Panasonic	ERJ-3GEYJ472V
R11	Resistor, chip, 2.49 kΩ, 1/10 W, 1%	0603	1		Vishay	CRCW06032K49FKEA
R12, R18, R19	Resistor, chip, 10 kΩ, 1/16 W, 5%	0603	3		Panasonic	ERA-V15J103V
R13	Resistor, chip, 150 kΩ, 1/10 W, 1%	0603	1		Vishay	CRCW0603150KJNEA
R15	Resistor, chip, 1 MΩ, 1/10 W, 1%	0603	1	open	Vishay	CRCW06031M00FKEA
R16	Resistor, chip, 20 kΩ, 1/10 W, 1%	0603	1		Vishay	CRCW060320K0FKEA
R17	Resistor, chip, 10 Ω, 1/16 W, 1%	0603	1	open	Vishay	CRCW060310R0FKEA
J11	Header, 2 position, Male	2mm	1	open	Norcomp	2163-36-01-P2

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#### **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the input voltage range of 10 V to 30 V and the output voltage range of 0 V to 30 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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